Remarks

Upon entry of the foregoing amendment, claims 1-6 and 9-12 are pending in the application, with claims 1, 6, and 12 being the independent claims. Reconsideration of this Application is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Claims 1, 3, 4, 6 and 12 have been editorially amended.

Claims 1-7 and 9-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo in view of Kean. Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo in view of Kean and Kawashima. Claims 7 and 8 have been canceled, and the subject matter of those claims have been incorporated into amended claims 1, 6, and 12. If the rejection of claim 8 is applied to the remaining claims as amended, the rejection is respectfully traversed for the following reasons.

As amended, claims 1, 6, and 12 call for a plurality of I/O buffers surrounding the functional blocks and the gate array block.

1. <u>The Office Action fails to provide a motivation for combining Dangelo and Kean.</u>

Dangelo discloses an integrated circuit that includes both core blocks (302, 304, 306, 308) and "customer logic". (Dangelo, Fig. 4 and associated description in col. 5, line 23 - col. 6, line 9) Kean is directed to a field programmable gate array of cells arranged in rows and columns. (Kean, for example, Fig. 7) The Examiner relies on Kean to teach that gate arrays are made up of basic cells and that basic cells can be arranged in a line. Otherwise, Kean adds nothing to the teachings of Dangelo. Furthermore, the Office Action fails to provide a motivation for combining Dangelo and Kean. There must be some suggestion of motivation to modify the reference or combine reference teachings. Since the Office Action has failed to provide such a motivation, a prima facie case of obviousness has not been established.

2. The prior art references of Dangelo and Kawashima are not properly combined.

Kawashima is cited by the Office Action as teaching I/O buffers at the chip edges. For example, Fig. 4A of Kawashima shows buffers 12 on the edges of the chip. The Office Action provides that the motivation for modifying Dangelo with the I/O buffers at the chip edges is "to achieve design flexibility as noted in the Kawashima abstract". The object of Kawashima is to provide design flexibility. However, Kawashima does not teach that design flexibility is achieved by placing the I/O buffers at the chip edges. Instead, Kawashima discloses buffers which are indistinguishably formed so as to be usable when either input buffers or output buffers are to constructed. (Kawashima, col. 3, lines 33-36) In Kawashima, design versatility is accomplished because the buffers can have functions set at will as either input or output buffers. (Kawashima, col. 3, lines 53-57; col. 6, lines 32-61; and col. 7, lines 1-7) Since Kawashima does

not teach that having I/O buffers on the chip edges accomplishes design flexibility, one skilled in the art would not think to combine the two references in the manner or for the purpose proposed by the Office Action.

3. Dangelo teaches away from the proposed modification, and the proposed modification of Dangelo would change its principle of operation.

One skilled in the art would not think to modify the structure taught in Dangelo with I/O buffers surrounding the functional and gate array blocks. Dangelo shows that the core is located in a central portion of the chip. (Dangelo, Figs 2 and 4) Furthermore, Dangelo states "I/O pads or ports are designed into each core", not that I/O pads can be formed anywhere else, such as the periphery. (Dangelo, col. 5, lines 11-14) Thus, Dangelo teaches that the I/O buffers are designed into each core in the central portion of the chip, and that the customer logic is formed on the periphery. (Dangelo, col. 5, lines 39-49) Dangelo emphasizes the advantage obtained by designing the customer logic on the periphery in that it enables easy redesign and revisions. (Dagelo, col. 5, line 66 - col. 6, line 9) Thus, Dangelo actually teaches away from Applicants' claimed method wherein I/O buffers are placed on the periphery.

Since Dangelo specifically teaches that the I/O buffers are designed into each core and that the customer logic is located on the periphery, locating the I/O buffers on the periphery would change the principle of operation of the integrated circuit of Dangelo. If the proposed modification or combination of the prior art references would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient

to render the claims prima facie obvious. (See MPEP 2143.01) Since a prima facie case of obviousness has not been established, it is respectfully requested that the rejection be withdrawn.

Applicants respectfully submit that because the amended claims and associated arguments overcome the rejections of the final Office Action, the Amendment places the application in condition for allowance. Further, it is submitted that the Amendment does not raise issues of new matter or present new issues requiring further consideration or search. Accordingly, Applicants respectfully request that this Amendment be entered.

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

A Notice of Allowance with claims 1-6 and 9-12 is respectfully requested.

Respectfully submitted,

Date: May 22, 2001

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Version with markings to show changes made

1. (Twice Amended) A method of manufacturing a semiconductor integrated circuit comprised of a plurality of functional blocks and a gate array block, each of the plurality of functional blocks being respectively provided with predetermined functions by semiconductor devices, the method comprising the steps of:

placing the gate array block comprised of a plurality of basic cells arranged in line and the plurality of functional blocks within a predetermined first area including a center position on a surface of a semiconductor chip;

placing a plurality of I/O buffers in a second area surrounding the first area;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells within the gate array block by using interconnections according to the circuits designed in the previous step.

3. (Twice Amended) A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein said step of placing the gate array block comprised of a plurality of basic cells arranged in line and the plurality of functional blocks within a predetermined first area including a center position on a surface of a semiconductor chip includes [first step is laid out]

laying out the gate array block and the plurality of functional blocks by one of a standard cell system and a full custom system.

4. (Twice Amended) A method of manufacturing a semiconductor integrated circuit according to claim 2, wherein said step of placing the gate array block comprised of a plurality of basic cells arranged in line and the plurality of functional blocks within a predetermined first area including a center position on a surface of a semiconductor chip includes [first step is laid out]

laying out the gate array block and the plurality of functional blocks by one of a standard cell system and a full custom system.

6. (Twice Amended) A semiconductor integrated circuit comprising:

a plurality of functional blocks placed on a semiconductor chip, said functional blocks being respectively provided with predetermined functions by semiconductor devices; [and]

a gate array block placed on said chip, said gate array block being comprised of a plurality of basic cells arranged in line and electrically connected between the basic cells lying within the gate array block by interconnections implementing a desired function, the gate array block having a circuit designed after placing said plurality of functional blocks and said plurality of basic cells on said chip,

wherein said functional blocks and said gate array block are laid out in a first area including a center position on a surface of the semiconductor chip; and

a plurality of I/O buffers surrounding the first area.

12. (Amended) A method of manufacturing a semiconductor integrated circuit comprising a plurality of functional blocks and a gate array block, each of said plurality of functional blocks being respectively completed by a layout design, the method comprising the steps of :

placing the gate array block, comprised of a plurality of basic cells arranged in line, within a first area of a semiconductor chip and said plurality of functional blocks within a second area of said semiconductor chip;

placing a plurality of I/O buffers in a third area surrounding the first and second areas;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells lying within the gate array block by using interconnections in accordance with the designed circuits whereby said designed circuits are formed on said semiconductor chip.

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